Appl. No. : **10/603,426**
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AMENDMENTS TO THE SPECIFICATION

Please replace paragraph number [0143] of the filed specification (number [0168] of the publication) with the following rewritten paragraph:

Subsequently the patterned resist is stripped. The oxide layer on top of the exposed first polysilicon layer 3 is removed. Then the first polysilicon layer 3 is etched self-aligned using the patterned first 4 and second 5 hard mask region to protect the underlying first polysilicon layer 3. As the second hardmask 5 is also polycrystalline silicon the spacer formed in the 2nd polysilicon layer 9 to define the program lines 33a-f as discussed in the previous embodiments of this aspect is removed while etching the first poly layer 3. Simultaneously, the patterned second poly ~~9~~5 is removed in the contact pad areas 41 while also defining the size of these areas. Then, the junctions 6 are implanted selfaligned to the patterned first polysilicon layer 3 in order to form the bitlines 6 as shown in figure 8c.

Please replace paragraph number [0146] of the filed specification (number [0171] of the publication) with the following rewritten paragraph:

The exposed gate dielectric ~~60~~2 is also removed. This is the gate dielectric at the bottom of the cavity 61 created by removing the first patterned hard mask 4 and the underlying first polysilicon layer 3. A second gate dielectric is deposited which could be an oxide or again a combined ONO layer for the case of a quadruple-bit cell as discussed in the fourth and fifth embodiment of the present invention. A next, i.e. third, polysilicon layer is deposited on top of the substrate. This second gate electrode material or third polysilicon layer is patterned to form the wordline 80 of the dual-bit structure in a fully self-aligned manner in a direction perpendicular to the bitlines 6 as discussed in previous embodiments of this aspect and as shown in figure 8f.